IN THE CLAIMS

1 (Currently Amended). A method comprising:

scaling a first portion and a second portion of image information to provide a scaled first portion and a scaled second portion that fit entirely within an addressable first memory area, wherein unscaled said first portion would substantially fill the ~~a~~ first memory area; and

storing said scaled first portion and said scaled second portion entirely in said first memory area.

2 (Currently Amended). The method of claim 1, further comprising:

accessing the scaled first or second portion from the first memory area;

retrieving a data sample from one of the scaled ~~portion~~ portions; and

using the data sample in a second scaling operation.

3 (Previously Presented). The method of claim 1, further comprising:

dividing a memory into a plurality of lines;

identifying a line; and

storing a number of scaled portions in the line, wherein scaling the first portion and the second portion is based on a scaling ratio, and the number is related to the scaling ratio.

4 (Currently Amended). A system comprising:

a memory comprising a number of bytes;

a scaler to perform a scaling operation, the scaling operation identifiable by a scaling ratio, wherein the scaler scales a first portion and a second portion of image information to provide a scaled first portion and a scaled second portion that fit entirely within addressable two-memory area, and unscaled said first portion would substantially fill the ~~a~~ first memory area; and

a memory controller coupled to the memory to store said scaled first portion and said scaled second portion entirely in said first memory area.

5 (Previously Presented). The system of claim 4, wherein the image information is a video data stream.

6 (Previously Presented). The system of claim 5, wherein the image information comprises a plurality of frames and each frame comprises a predetermined number of bytes.

7 (Original). The system of claim 6, wherein the number of bytes in the memory is smaller than the predetermined number of bytes.

8 (Original). The system of claim 4, wherein the scaling operation is a horizontal scaling operation.

9 (Previously Presented). The system of claim 4, further comprising:

a second scaler to perform a second scaling operation, identifiable by a second scaling ratio.

10 (Original). The system of claim 9, wherein the second scaling ratio is identical to the first scaling ratio.

11 (Original). The system of claim 9, wherein the second scaling operation is a vertical scaling operation.

12 (Original). The system of claim 9, further comprising:

a scaling control unit coupled to the second scaler, wherein the second scaler further comprises a finite impulse response filter including a plurality of coefficients and the scaling control unit changes the amount of coefficients in the filter in relation to the scaling ratio.

13 (Original). The system of claim 12, wherein the scaling control unit further comprises a look-up table including coefficient values for changing the amount of coefficients.

14 (Original). The system of claim 4, further comprising a first-in-first-out memory.

15 (Original). The system of claim 4, wherein the memory is an on-chip memory.

16 (Currently Amended). An article comprising a medium storing instructions that, if executed, enable a processor-based system to:

scale a first portion and a second portion of image information to provide a scaled first portion and a scaled second portion that fit entirely within an addressable first memory area, wherein unscaled said first portion would substantially fill a first memory area; and

store said scaled first portion and said scaled second portion entirely in said first memory area.

17 (Currently Amended). The article of claim 16, further storing instructions that, if executed, enable a processor-based system to:

access ~~a~~ the scaled first or second portion from the first memory area;

retrieve a data sample from one of the scaled ~~portion~~ portions; and

use the data sample in a second scaling operation.

18 (Previously Presented). The article of claim 16, further storing instructions that, if executed, enable a processor-based system to:

divide a memory into a plurality of lines;

identify a line of the plurality of lines; and

store a number of scaled portions in the line, wherein scaling the first portion and the second portion is based on a scaling ratio, and the number is related to the scaling ratio.